REMARKS

Claims 1-20 are pending in the case. All claims stand rejected. In the present submission, claims 1, 11, 12 and 16-18 have been amended and claims 10 and 20 have been cancelled. Applicant has also amended the specification to update a reference to a related application and to correct a typographical error. Reconsideration is respectfully requested.

Specification Amendment

The application has now been amended to update the reference to the related application in paragraph [0002], as requested by the Examiner.

Double Patenting

Claims 1-20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-21 of copending patent application serial no. 10/759,786 in view of Ishida (U.S. Patent 5,504,697). Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c). Withdrawal of the provisional double patenting rejection is respectfully requested.

§103 Rejection

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelly (U.S. Patent 5,942,992) in view of Ishida (U.S. Patent 5,504,697). Applicant respectfully traverses the rejection.

Kelly describes an engineering unit converter system for converting an analog measurement into an engineering value. The analog measurement is digitized and the digital value is split into a high order digital and a low order digit. "The high order digit is used as an address to a memory device for fetching a line segment coefficient and a line segment offset coefficient. The lower order digit is multiplied with the line segment coefficient in a multiplier resulting in a product. The product is added to the line segment coefficient offset resulting in a sum whose value is an engineering unit." (See Abstract of Kelly). See also Kelly, col. 4, ln. 42-54.) Kelly in col. 5, ln. 22-24 further describes the "high order bits 208 act as an address 212 and the low order bits 218 remain in a data state as a portion of the digital value 204 coming out of the ADC 202."

Ishida describes a limiter circuit for limiting an output data to a limit value when an input data exceeds in value the limit value. (See Abstract of Ishida.)

Claim 1

Claim 1, as amended, recites:

> 1. A device for performing numerical value conversion of a digital **an N-bit digital input value** in a first unit to a second unit being a natural unit, the first unit being related to the second unit by a first equation, the digital input value being a digitized value of a first measurement parameter among a plurality of measurement parameters, the device comprising:
>
> a memory having stored thereon a look-up table storing a plurality of coefficients for performing the numerical value conversion from the first unit to the second unit for each of the plurality of measurement parameters, **the look-up table being indexed using a first parameter to provide a selected coefficient, the first parameter being indicative of the first measurement parameter**;
>
> an arithmetic logic unit **receiving the N-bit digital input value** in the first unit and the selected coefficient from the look-up table, the arithmetic logic unit performing the numerical value conversion based on the first equation and using the selected coefficient to compute a digital output value in the second unit; and
>
> a saturation-limit circuit coupled to receive the digital output value in the second unit from the arithmetic logic unit and provide a predetermined final output value when the digital output value exceeds a predetermined minimum or maximum value. (Emphasis added.)

Claim 1 is patentable over the cited references at least by reciting "the look-up table being indexed using a first parameter to provide a selected coefficient, the first parameter being indicative of the first measurement parameter" and "an arithmetic logic unit receiving the N-bit digital input value in the first unit."

In the claimed invention of claim 1, the device for performing numerical value conversion is capable of converting a digital input value selected from "a plurality of measurement parameters." As explained in Applicant's specification, paragraphs [0048] to [0052], the numerical value conversion device can be used to convert digital input values from multiple data sources. To that end, the lookup table is indexed by a "first parameter" that is indicative of the selected "measurement parameter," as recited in claim 1 and explained

in paragraphs [0051]-[0052] of Applicant's specification. The first parameter in claim 1 is analogous to the indexing parameter P2 of Figure 7. By using the first parameter to index the look-up table, coefficients associated with the selected measurement parameter is provided to the arithmetic logic unit. This limitation of claim 1 is not taught by Kelly or Ishida. Kelly describes merely using the higher order bits to index the memory to fetch the coefficients. Kelly does not describe storing coefficients for different measurement parameters and using an index associated with the selected measurement parameter to index the look-up table, as recited in claim 1.

Furthermore, the claimed invention of claim 1 uses the first parameter to select the coefficients and then the entire N bits of the digital input value is being processed to convert the N-bit digital input value to the digital output value in the second, natural unit. Kelly does not teach or describe processing the entire N bits of the digital input value. Rather, Kelly describes selecting coefficients for the engineering unit conversion using the high order bits as address. Kelly performs numerical value conversion only on the low order bits which are used as data.

For at least these reasons, claim 1 is patentable over Kelly. Ishida does not cure the deficiency of Kelly. Therefore, claim 1 is patentable over Kelly or Ishida, alone or in combination.

Claims 2-11

In the present submission, claim 10 has been cancelled and the rejection as to this claim is moot.

Claims 2-9 and 11, dependent upon claim 1, are patentable over Kelly and Ishida at least for the same reasons that claim 1 is patentable.

Claim 11 is patentable over the cited references for the additional reasons that Kelly does not teach or describe "the digital input value comprises a plurality of digital input values, each digital input value being provided to the device for performing numerical value conversion, the plurality of digital input values comprising at least a first digital input value of a first bit length and a second digital input value of a second bit length different than the first bit length." The numerical value conversion device of the present invention is capable of operating on digital input values having variable bit lengths. Kelly specifies Y number of

higher order bits for addressing and X number of lower order bits for data conversion. Neither Kelly nor Ishida teaches or describes that the digital input data can have different bit lengths. Claim 11 has been amended to further clarify the claim.

Claims 12-20

In the present submission, claim 20 has been cancelled and the rejection as to this claim is moot.

Claim 12 is patentable over the cited references at least by reciting "indexing the look-up table using a first parameter being indicative of the first measurement parameter to provide a selected coefficient" and "providing the N-bit digital input value and the selected coefficient to an arithmetic logic unit." For the same reasons stated above with reference to claim 1, Kelly fails to teach addressing the coefficient table using a first parameter that is indicative of the selected measurement parameter of the digital input value. Also, Kelly fails to teach providing all N bits of the digital input value for numerical value conversion.

For at least these reasons, claim 12 is patentable over Kelly. Ishida does not cure the deficiency of Kelly. Therefore, claim 12 is patentable over Kelly or Ishida, alone or in combination.

Claims 13-19, dependent upon claim 12, are patentable over Kelly and Ishida at least for the same reasons that claim 12 is patentable.

Claim 16 is patentable over the cited references for the additional reasons that the cited references do not teach or describe "the digital input value comprises a plurality of digital input values, each digital input value being provided for performing numerical value conversion, the plurality of digital input values comprising at least a first digital input value of a first bit length and a second digital input value of a second bit length different than the first bit length", as discussed above with reference to claim 11. Claim 16 has been amended to further clarify the claim.

For the reasons stated above, claims 1-9 and 11-19 are patentable over the cited references. Withdrawal of the §103(a) rejection of the claims is respectfully requested.

CONCLUSION

Claims 1-20 are pending in the present application. Claims 1, 11, 12 and 16-18 have been amended and claims 10 and 20 have been cancelled. The specification has been amended to correct typographical error and to update references to related application. No new matter has been entered. For the reasons stated above, the application is in condition for allowance and passage of the present case to allowance is respectfully requested. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

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/Carmen C Cook/	May 9, 2007
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,

/Carmen C Cook/

Carmen C. Cook
Attorney for Applicant(s)
Reg. No. 42,433
Patent Law Group LLP
2635 N. First St.
Suite 223
San Jose, CA 95134
Tel (408) 382-0480 x208
Fax (408) 382-0481